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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,095	08/25/2000	Akella V.S. Satya	KLA1P016F	4627

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/648,095	Applicant(s) SATYA ET AL.	
	Examiner Quang D Vu	Art Unit 2811	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 06/02/03 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *7,54-60 and 107*.

   Claim(s) withdrawn from consideration: _____.
8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Steven Lake
Primary Examiner

Steven Lake

Continuation of 5. does NOT place the application in condition for allowance because: Claims 7, 54 and 107 are rejected under 35 U.S.C. 112, first paragraph for the reason in record paper #11. Claim 58 is objected under specification for the reason in record paper #11.

It is argued, in page 2 of the remarks, that the specification discloses dummy fillings can be fabricated as contacts between a metal layer under test and the substrate and a defect is detected when a contact is open since it appears dark as compared with a coupled contact which appears light (i.e, emits secondary electrons). This argument is not convincing because the specification only discloses the dummy fillings can be fabricated to prevent defects caused by CMP polishing on page 44.

It is argued, in page 2 of the remarks, that the voltage contrast testing of such of structure is described in detail at page 32, 2nd paragraph through page 33, 2nd paragraph with respect to fig. 7a. This argument is not convincing because fig. 7a belongs to the other embodiment.

It is argued, in page 3 of the remarks, that the specification teaches determining whether one or more empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing on page 44, 3rd paragraph. This argument is not convincing because the specification only discloses "after the test chip is initially designed, it may be determined whether empty space requires dummy fillings to prevent defects caused by CMP polishing" on page 44. The specification also never discloses the empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing.

It is argued, in page 3 of the remarks, that the specification discloses the dummy filling coupled to the test structure. This argument is not convincing because the specification never discloses the dummy filling coupled to the test structure.

It is argued, in page 4 of the remarks, that the testing of such a structure is fully discribed at page 32, 2nd paragraph through page 33, 2nd paragraph with respect to fig. 7a. This argument is not convincing because fig. 7a belongs to the other embodiment. The specification never discloses a first test structure and a second test structure, wherein the first test structure is coupled with the substrate of the semiconductor die and the second test structure is not and wherein at least one of the dummy fillings is coupled to the first test structure and at least one of the dummy filling is coupled to the second test structure; performing voltage contrast inspection on the first and second test structures to detect a defect within the first and second test structure, wherein a defect is detected when the first test structure differs from a voltage potential of the second test structure.

It is argued, in page 4 of the remarks, that the specification discloses all the claimed limitation in claim 54. This argument is not convincing because the specification never discloses one or more empty spaces that are positioned outside the first areas require dummy fillings to facilitate an even polishing of a surface of the semiconductor die during CMP polishing. The specificaiton only discloses the empty space requires dummy fillings to prevent defects caused by CMP polishing.